In the Specification:

Please replace the paragraph starting on page 3, line 1, with the following:

A need exists for an improved imager cell that addresses the problems noted above and others previously experienced.

Please replace the paragraph starting on page 5, line 22, with the following:

~~In general, the p-doping may be accomplished using _____, while the n-doping may be accomplished using _____, and the p++ doped pinned region 220 may be formed by _____.~~ Note that the transfer gate 206 is disposed between the photoreceptor 204 and the sense node 208 in order to transfer charge 'between the photoreceptor 204 and the sense node 208. Note also that the transfer gate 206 includes a transistor gate structure (i.e., the photoreceptor readout gate 216). As explained in more detail below, the imager cell 200 sets up a potential well profile that allows charge to transfer through the transfer gate 206 depending on photoreceptor control clocks.

Please replace the paragraph starting on page 6, line 8, with the following:

The operation of the imager cell 200 in low-light mode is now discussed with reference to the potential well diagram 214 and the photoreceptor control clock 228. Note that the photoreceptor control clock 228 varies between a V- level during an integration period 230 and a V+ level during a readout period 232. The duration of the integration period 230 and the readout period 232 vary in accordance with the desired operating speed of the imager cell 200. ~~In one implementation, for example, the duration of the integration period 230 is approximately _____, while the duration of the readout period 232 is approximately _____.~~

Please delete the paragraph starting on page 7, line 18, as follows:

~~In particular, the controller 302 may by constructed as _____. JIM - INSERT MORE DETAIL ON HOW THE CONTROLLER IS IMPLEMENTED - IS IT A PROCESSOR CORE, OR ALL CUSTOM LOGIC?~~

Please replace the paragraph starting on page 7, line 19, with the following:

Typically, the controller 302 operates the imager 300 in the low-light mode. In the low-light mode, the controller 302 asserts the photoreceptor control clock 228 as noted above. In particular, the controller 302 asserts a photoreceptor control clock with an integration period ~~224~~ 230 and a readout period ~~222~~ 232. Thus, the photoreceptor potential well 234 provides the charge capacity to accumulate electrons produced by incident photons. The charge capacity is generally sufficient for imaging in low-light levels. In other words, the controller 302 selects the low-light mode when the controller 302 determines (or is explicitly commanded by an operator through input keys) that the measured, predicted, or modeled quantum efficiency and charge capacity of the ~~charge collection~~ photoreceptor potential well 234 will not be overwhelmed by electrons generated based on current lighting conditions.

Please replace the paragraph starting on page 10, line 3, with the following:

Note that during high-light mode as the integration voltage V+ increases, so does the depth of the potential well 240, and thus so does the overall charge capacity level for the photoreceptor ~~202~~ 204. As a result, during conditions of bright light, for example, the controller 302 may increase the integration voltage V+ to enhance the charge collection capacity level in the photoreceptor ~~202~~ 204 (and thereby reduce blooming or washout, as examples). To that end ,

the controller 302 may be preprogrammed with a selection of V+ integration voltages to apply, during high-light mode, to the photoreceptor readout gate 216, as selected by external input, or in coordination with measurements received from external light sensors or the like.

Please replace the paragraph starting on page 10, line 12, with the following:

As noted above, the imager cell 200 may also operate in what is referred to as a "Snap" mode in conjunction with the low-light mode. In the Snap mode, the controller 302 asserts the V+ readout voltage 232 of the photoreceptor control clocks 306 for multiple imager cells 200 simultaneously. The result is that the charge collected in a set of photoreceptors ~~200~~ 204 is simultaneously transferred into the sense nodes 208 of each respective photoreceptor 204. The Snap mode thus provides a snapshot at an instant in time of the charge collected in the set of photoreceptors ~~200~~ 204 to obtain image information undisturbed by noise arising during, for example, a sequential readout process.

Please replace the paragraph starting on page 10, line 21, with the following:

As an example, numerous imager cells 200 may be organized into an array to form a CMOS imager. The controller 302 may then select two or more imager cells 200 as a set of photoreceptors ~~200~~ 204 for the next Snap operation. As examples, the set may include all the photoreceptors ~~200~~ 204 that form a rectangular sub-array in the center of the CMOS imager, a stripe of predetermined width vertically through the center of the CMOS imager, or every other imager cell 200 in the CMOS imager.

Please replace the paragraph starting on page 11, line 14, with the following:

On the other hand, in the low-light mode, the controller 302 asserts (408) a V-integration voltage during an integration period. Electrons generated by incident photons are then collected in the photoreceptor potential well 234. In optional conjunction with Snap mode operation, the controller 302 then asserts (410) a V+ readout voltage to a set of photoreceptors ~~200~~ 204. Captured charge is thereby simultaneously transferred to the sense nodes 208 associated with each photoreceptor 204 that is part of the Snap operation. It is noted that it is not necessary to use the Snap mode, however. In other words, conventional photoreceptor array readout techniques are also suitable.